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PATENT

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September 7, 1999 — Edward W. Bulchis
Date — Edward W. Bulchis

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Brent Keeth
Application No.	:	08/798,227
Filed	:	February 11, 1997
For	:	MEMORY SYSTEM WITH DYNAMIC TIMING CORRECTION

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Examiner	:	David Ransom
Art Unit	:	2752
Docket No.	:	660073.587
Date	:	September 7, 1999

Attention: Board of Patent Appeals and Interferences
Assistant Commissioner for Patents
Washington, DC 20231

APPELLANT'S BRIEF (37 C.F.R. § 1.192)

Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on July 7, 1999. The fees required under Section 1.17(f), and any required request for extension of time for filing this brief and fees therefor, are dealt with in the accompanying transmittal letter.

The applicant, Brent Keeth, hereby appeals to the Board of Patent Appeals and Interferences from the decision of Examiner Ransom dated April 13, 1999 finally rejecting claims 1-24.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, Micron Technology, Inc., a Delaware Corporation having a place of business at Boise, Idaho.

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II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellant, the appellant's legal representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-24 remain in this application. All of these claims have been rejected for the reasons described below, and applicant is appealing from the rejections of these claims.

Claims 1-6, 8-1, 13-18 and 20-24 were finally rejected under 35 U.S.C. § 102(e) as being anticipated by U. S. Patent No. 5,577,236 to Johnson et al.

Claims 7, 12 and 19 were rejected under 35 U.S.C. § 103(a) as being obvious over the patent to Johnson et al. in view of U.S. Patent No. 5,020,023 to Smith.

IV. STATUS OF AMENDMENTS

Claims 1-15 were initially presented for examination and rejected in an Office Action dated April 30, 1998 (Paper No. 5) on essentially the same basis as in the final rejection except that claim 12 was rejected on the basis of the patent to Johnson et al. in view of U.S. Patent No. 5,692,165 to Jeddeloh et al. Applicant responded on July 20, 1998 amending some of the claims to make them clearer, adding new claims 16-19, and explaining how the claims patentably distinguished over the cited references. The Examiner maintained his rejection in an Office Action dated September 11, 1998 (Paper No. 7) except that claim 12 was now rejected on the same basis as in the final rejection.

Applicant's attorney subsequently conducted a telephone interview with Examiner Ransom on December 11, 1998. During the interview, agreement was reached that the claims patentably distinguished over the cited references and the application would be allowed unless more pertinent prior art could be found. This agreement is reflected in the Interview Summary[1] dated December 11, 1998 and in applicant's response filed December 11, 1998 making the substance of the interview of record and adding new claims

[1] The Interview Summary also contains a detailed description of the technical content agreed upon. However, applicant's attorney does not understand how these remarks relate in any manner to the claimed invention, although they seem to be an attempt to explain why the Johnson et al. patent fails to teach or suggest the claimed invention.

20-24. Despite the Examiner's agreement on the claims, he finally rejected the claims on the same basis as in the earlier Office Action.

V. SUMMARY OF THE INVENTION

The present invention is directed to solving the problem of precisely coupling digital signals, such as data, from a memory device to a memory controller. As the speed of memory devices continues to increase, controlling the timing at which data signals are received at the memory controller becomes more critical. Precisely controlling the timing at which data signals are received by a memory controller is even more difficult where, as in the disclosed embodiment, the memory controller communicates with several memory devices. In such cases, the timing of data signals generated by each memory device may be different and the time required for the data signals to propagate from each memory device may vary.

The disclosed embodiment of the invention will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and the subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Board appreciate important claim distinctions discussed thereafter.

The disclosed embodiment of applicant's invention solves the above-described problem by (1) determining the timing error at which a digital signal output from a memory device is received at the memory controller, (2) communicating the existence and/or magnitude of the error to the memory device that outputted the digital signal, and (3) adjusting the timing at which the next digital signal is output from the memory device so that the timing error at which it is received at the memory controller is reduced. Note that the timing adjustment is done at the memory device rather than at the memory controller, even though it is the timing of the digital signal at the memory controller that is critical. Thus, the memory device adapts itself to output the digital signal to the memory controller at the optimum time for the memory controller to capture the digital signal. This feature, which may be termed "adaptive signal timing", allows a memory system containing the memory controller and several memory devices to automatically configure itself for optimum performance.

In the disclosed embodiment, the memory controller generates a master clock signal that is coupled from the memory controller to the memory device. The memory device then uses the master clock signal to generate an echo clock signal. The phase of the echo clock signal relative to the master clock signal is determined by timing control data that is received from the memory controller. The echo clock signal is used to clock read data from the memory device, and this read data, as well as the echo clock, are coupled from the memory device to the memory controller. The memory controller then compares the phase of the received echo clock signal to the phase of the master clock signal to determine the timing error of the echo clock signal. Since the echo clock signal is used to clock the read data, the timing error of the echo clock signal also corresponds to the timing error of the read data as it is received by the memory controller. The memory controller sends timing control data indicative of the timing error to the memory device, and the memory device then adjusts the phase of the error clock signal relative to the phase of the received master clock signal accordingly. This timing adjustment reduces the timing error of the echo clock signal and the read data as they are received at the memory controller.

Various aspects of the disclosed embodiment described above are covered by the claims, as discussed in greater detail below.

VI. ISSUES

The following are the issues presented for review:

(1) whether the Examiner properly rejected claims 1-6, 8-1, 13-18 and 20-24 under 35 U.S.C. § 102(e) as being anticipated by U. S. Patent No. 5,577,236 to Johnson et al.

(2) whether the Examiner properly rejected claims 7, 12 and 19 under 35 U.S.C. § 103(a) as being obvious over the patent to Johnson et al. in view of U.S. Patent No. 5,020,023 to Smith.

VII. GROUPING OF CLAIMS

For purposes of this appeal, the claims can be grouped together for the purpose of considering the rejections based on 35 U.S.C. §§ 102 and 103 as follows:

(1) Independent claims 1, 6, 16 and 20, and dependent claims 3-5, 7, 9, 17, 19 and 22-24 can be grouped together and represented by claim 20;

(2) Dependent claims 2, 8, 18, 21, which are dependent on claims 1, 6, 16 and 20, respectively, can be grouped together and represented by claim 21;

(3) Independent claim 10, dependent claim 12, and independent claim 13 can be grouped together and represented by claim 10;

(4) Dependent claim 11, which is dependent on claim 10, and dependent claims 14 and 15, which are dependent on claim 13, can be grouped together and represented by claim 11.

VIII. ARGUMENT

1. The Cited References Are Not Pertinent To The Claimed Inventions

A. *The Johnson et al Patent*

With reference to Figure 3, the Johnson patent discloses a memory controller 302 having a system clock circuit 303 generating a system clock signal that is fed to a memory bank 300, and an inverted system clock signal, which is derived from the system clock signal, is fed to a command driver 308. The command driver 308 sends read commands to the memory bank 300, with the timing of the read commands determined by the system clock signal. See col. 5, line 47-col. 6, line 18.

The memory controller 302 described in the Johnson patent also has a sampling clock circuit 304 providing multiple sampling clock signals, each having a phase shift relative to the system clock signal. A multiplexer 307 selects one of the sampling clock signals to be fed to a delay module 313, the output of which is fed to a first receiver 319 that synchronizes a latch 322 to accept read data transmitted by the memory bank 300. See col. 6, lines 8-46. The delay module 313 includes an off-chip supplementary delay unit 316 of a fixed value. The delay value can be adjusted only by physically replacing the off-chip delay unit 316 with one having the desired delay value. See col. 6, line 53-col. 7, line 20.

Selection of which sampling clock signal to feed to the delay module 313 is based on information fed to the multiplexer 307 from a data source 305. The data may be a processor that is separate from the memory controller 302, which controls the multiplexer 307 to select the appropriate sampling clock signal from the sampling clock circuit based upon the type of memory bank, the number of memory device present in the memory bank, etc., all of which are a factor in delaying signals coupled between the memory bank 300 and the memory controller 302. See, col. 8 , lines 23-59. Alternatively, the data source 305 may be a set of

mechanical switches set by the user. See, col. 8, lines 60-64. Once the information in the data source 305 is established, the multiplexer 307 cannot select any other sampling clock signal until the information in the data source is either reprogrammed or manually changed. See col. 8, lines 41-44, and col. 8, lines 60-64.

Several key facts concerning the Johnson et al. system should be noted. First, the Johnson et al. system does not employ "adaptive signal timing" as described above to automatically configure the memory controller and memory to optimum performance. More particularly, the Johnson et al. memory controller does determine a timing error of the data signal on line 320 and then make any adjustments to reduce the timing error. Although the multiplexer 307 can select differently phased sampling clock signals, the multiplexer 307 does not do so based on a measured timing error as in applicant's system. Second, the adjustment made by the multiplexer 307 is performed in the memory controller rather than in the memory devices. In applicant's system, the memory controller sends control data to each memory device indicative of the timing error of a digital signal received from each memory device. Thus, each memory device can configure itself so that digital signals, such as data, generated by the memory device is received by the memory controller at the same time relative to the system clock regardless of which memory device has generated the digital signal. This is not possible in the Johnson et al. system.

Thus, the Johnson et al. patent does not disclose a structure or operation where the memory controller 302 identifies a phase error between a signal transmitted from the memory device and a clock signal of the memory controller 302, and then transmits data to the memory bank 300 in order to cause the memory bank 300 to revise the timing at which it outputs data.

B. *The Smith Patent*

The Smith patent discloses a system using a FIFO buffer and a technique of marking "frames" of a data stream to remove skew between multiple correlated synchronous data streams. See col. 5, line 40-col. 7, line 15. Data is placed into a FIFO register with the frame encoding and then removed from the FIFO buffer when the data is to be consumed. If a synchronization fault is detected when the data is unloaded from the FIFO buffer, a re-synchronization procedure is triggered. The procedure described in the Smith patent entails: inhibiting the unloading and loading of the FIFO buffer, purging the FIFO buffer, reloading

data into the FIFO buffer while monitoring for the next frame mark, and when the next frame mark is detected, re-enabling normal loading and unloading of the FIFO buffer where unloading starts with the frame marked data. See col. 6, line 60-col. 7, line 15, and Figure 5.

2. The Claims Represented By Independent Claim 20 Patentably Distinguish Over The Cited References

Claim 20, which is representative of independent claims 1, 6, 16 and 20, and dependent claims 3-5, 9, 17 and 22-24, is not anticipated by the Johnson et al. patent, nor are claims 7 and 19 taught or suggested by the Johnson et al. patent either alone or in combination with the Smith patent.

Claim 20 specifies a method of adjusting data timing in a memory system having a memory device and a memory controller. According to the claimed method, an initial output timing at the memory device is established and is then subsequently revised. The output timing is revised by "transmitting a first digital signal from the memory device to the memory controller according to the initial output timing." After the echo clock signal is received at the memory controller, the memory controller identifies "a phase difference of the received echo clock signal relative to a timing reference signal" and "transmits an adjustment signal to the memory device for revising the initial output timing in response to the identified phase difference to produce a revised output timing." Thereafter, the memory device revises the initial output timing according to the adjustment signal. The memory device then transmits a second digital signal from the memory device to the memory controller according to the revised output timing.

As explained above, the Johnson et al. patent does not disclose a memory controller that identifies a phase error between a received digital signal relative to a timing reference signal, as recited claim 20. Nor does the Johnson et al. system transmit an adjustment signal to the memory device to cause the memory device to revise the initial output timing. Finally, the Johnson et al. patent does not disclose any system in which the timing of a signal generated by a memory device can be adjusted. Instead, the only signal having its timing adjusted in the Johnson et al. system is selecting one of several sampling clock signals, but this selection is done in the memory controller and not in the memory device, as in applicant's system.

The Johnson et al. system thus not only fails to include individual components that operate as claimed, but these components do not operate together in any manner that is at all similar to the method of claim 20. Basically, the Johnson et al. system does not have any "adaptive signal timing" capability.

Claim 7 and 19 have been rejected under 35 U.S.C. 103(a) as being obvious over Johnson et al. in view of Smith. Claim 7, which is dependent on claim 6, and claim 19, which is dependent on claim 16, add the limitation of adjusting a vernier to select the adjusted time delay. After the memory device transmits an echo clock signal to the memory controller, the echo clock signal and the master clock signal are compared to determine their relative phase difference. Adjustment of the vernier is made based on the relative phase error determined from the comparison.

The deficiencies of the Johnson reference, as discussed above, are not made up for by the Smith patent. The Smith patent uses the term "Vernier Synchronization" and "Vernier Skew compensation" to simply describe the fact that frame synchronization used by the disclosed system may be made by adjusting in increments of fractional frame skew, as compared to whole frame synchronization. See col. 7, lines 16-21. Smith's use of "vernier" has nothing to do with disclosing or suggesting adjusting a vernier in adjusting a time delay in response to the relative phase relationship between two signals. Smith's reference to "vernier" simply describes making adjustments in less than whole increments.

3. The Claims Represented By Dependent Claim 21 Patentably Distinguish Over The Cited Reference

Claim 21, which is representative of dependent claims 2, 8, 18 and 21, is not anticipated by the Johnson et al. patent. Claim 21 specifies the manner in which the step recited in claim 20 of identifying a phase difference of the first digital signal relative to a timing reference signal is accomplished. According to the claimed method, a plurality of phase shifted signals are generated responsive to the timing reference signal. The first digital signal is then compared to each of the phase shifted signals. Finally, one of the phase shifted signals having a phase within a selected range relative to the digital signal is identified.

The only "plurality of phase shifted signals" disclosed in the Johnson et al. patent are the sampling clock signals generated by the sampling clock circuit 304. But these sampling clock signals are not compared to any other signal in any manner. Instead, one of

these sampling clock signals is selected by the multiplexer 307. The Johnson et al. patent thus fails to anticipate the subject matter of claim 21.

4. The Claims Represented By Independent Claim 10 Patentably Distinguish Over The Cited References

Claim 10, which is representative of independent claims 10 and 13 and dependent claim 12, is not anticipated by the Johnson et al patent, nor is claim 12 suggested by the Johnson et al. patent either alone or in combination with the Smith patent.

Claims 10 and 13 are directed to a memory controller and a memory system, respectively,. Claim 10 specifies memory devices that produce echo signals in response to master clock signals applied to a clock bus from a master clock source in the memory controller. The memory controller includes a phase comparing circuit that produces a phase signal in response to a phase difference between the echo signal and the master clock signal. The claim further specifies that the memory controller includes a logic circuit that produces adjustment data in response to the phase signal, and a control data circuit adapted to produce a command signal in response to the adjustment data.

The Johnson system does not anticipate the subject matter of claim 10. More specifically, the Johnson system does not have a phase comparing circuit which compares the phase difference between a signal transmitted by the memory device and a clock signal of the memory controller. The system shown in Figure 3 and described in col. 5, line 19-col. 7, line 40 does not include a phase comparing circuit that compares the phase error between a clock signal transmitted from the memory bank to the memory controller or a logic circuit that produces a signal in response to the output of the phase comparing circuit. What is shown and described is a system where a clock signal is selected by providing to a multiplexer predetermined information encoded in a hardware data source. None of the clock signals can be modified (i.e., the relative phase relationship of the output of the sampling clock is fixed) nor can the selection of which clock signal to transmit to the delay module be changed unless the predetermined information from the hardware data source is reprogrammed or manually switched. Furthermore, additional delay of the selected clock signal is possible only by inserting a fixed, off-chip delay unit into the signal path; the delay value can only be modified by replacing that fixed delay unit with another fixed delay unit having a different delay value.

For the foregoing reasons, claim 10 is not anticipated by the Johnson et al. patent.

5. Dependent Claim 11 Patentably Distinguish Over The Cited Reference

Claim 11, which is dependent on claim 10, and claims 14-15, which are dependent on claim 13, are represented by claim 11. Claim 11 is directed to the phase comparator of claim 10, and it specifies a signal source operative to produce a plurality of phase shifted signals in response to the master clock signal. A plurality of phase comparators then compare the echo signals to each of the phase shifted signals present at a respective input.

As explained above in section 3, the only "plurality of phase shifted signals" disclosed in the Johnson et al. patent are the sampling clock signals, which are not compared to any other signals. For these reasons, the claims represented by claim 11 are not anticipated by the Johnson et al. patent.

IX. APPENDIX

Attached hereto is a copy of pending claims 1-24, which are involved in this appeal.

Respectfully submitted,
Brent Keeth
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APPENDIX

1. A method of adjusting data timing in a memory system having a memory device and a memory controller, the system operating according to a master clock signal, the method comprising the steps of:

establishing an initial output timing at the memory device;

transmitting an echo clock signal from the memory device to the memory controller according to the initial output timing;

receiving the echo clock signal at the memory controller;

identifying a phase error of the received echo clock signal relative to the master clock signal;

transmitting control data from the memory controller to the memory device for revising the initial output timing in response to the identified phase error to produce a revised output timing;

revising the initial output timing of the memory device according to the control data; and

transmitting a second set of data from the memory device to the memory controller according to the revised output timing.

2. The method of claim 1 wherein the step of identifying a phase error of the received echo clock signal relative to the master clock signal comprises the steps of:

generating a plurality of phase shifted signals responsive to the master clock signal;

comparing the echo clock signal to each of the phase shifted signals; and

identifying one of the phase shifted signals having a phase within a selected range of phases relative to the echo clock signal.

3. The method of claim 2 wherein the step of establishing an initial output timing includes the steps of:

setting a delay of a delay circuit; and

applying the master clock signal to the delay circuit to produce the echo clock signal.

4. The method of claim 3 wherein the step of establishing an initial output timing further includes the steps of:

storing data in an output register;

clocking the register with the echo clock signal; and

outputting data from the register in response to the echo clock signal.

5. The method of claim 3 wherein the step of revising the initial output timing includes the step of adjusting the delay of the delay circuit.

6. A method of controlling data flow in a memory system including a memory controller and a memory device, the method comprising the steps of:

generating a master clock signal;

transmitting the master clock signal from the memory controller to the memory device;

issuing a first read command to the memory device;

producing an echo signal at the memory device in response to the first read command, the echo signal having a phase shift relative to the master clock signal;

transmitting the first set of data to the memory controller with a time delay relative to the echo signal;

transmitting the echo signal to the memory controller;

receiving the echo signal at the memory controller;

comparing the received echo signal to the master clock signal;

selecting an adjusted time delay in response to the step of comparing the received echo signal to the master clock signal;

issuing a second read command to the memory device;

reading a second set of data in response to the second read command; and

transmitting to the memory controller the second set of data with the adjusted time delay.

7. The method of claim 6 wherein the step of selecting an adjusted time delay includes the step of adjusting a vernier.

8. The method of claim 6 wherein the step of comparing the received echo signal to the master clock signal includes the steps of:

producing a plurality of phase-shifted signals in response to the master clock signal; and

comparing the echo signal to each of the phase-shifted signals.

9. The method of claim 8 wherein the step of selecting an adjusted time delay includes the step of identifying one of the phase-shifted signals closest in phase to the echo clock signal.

10. A memory controller for a memory system including a plurality of memory devices coupled to common clock and command busses, the memory devices producing echo signals in response to clock signals on the clock bus, the controller comprising:

a master clock source coupled to the clock bus operative to produce a master clock signal;

a phase comparing circuit coupled to the clock bus and responsive to produce a phase signal in response to a phase difference between the echo signal and the master clock signal;

a logic circuit coupled to the phase comparing circuit and adapted to produce adjustment data in response to the phase signal; and

a control data circuit having a command output coupled to the command bus and adapted to produce a command signal at the command output in response to the adjustment data.

11. The memory controller of claim 10 wherein the phase comparator includes:

a signal source having a plurality of outputs and operative to produce a plurality of phase-shifted signals at the outputs in response to the master clock signal; and

a plurality of phase comparator, each phase comparator including a first input coupled to the signal source outputs, a second input coupled to the clock bus to receive echo signals and a phase output coupled to the logic circuit.

12. The memory controller of claim 11 wherein the signal source includes a multiple output delay-locked loop.

13. A memory system, comprising:

a command bus;

a clock bus;

a data bus;

a memory controller including a master clock generator coupled to the clock bus to generate a master clock signal, a phase comparator having a first input coupled to the master clock generator and a second input and responsive to a phase difference between the first and second inputs to produce an adjust command, and a logic circuit; and

a memory device having a clock input coupled to the clock bus, an echo signal generator to generate an echo signal responsive to the master clock signal at the clock input, the echo signal generator being coupled to the second input of the phase comparator, a data latch having a trigger input and responsive to a control signal at the trigger's input to transmit data to the data bus, and a variable delay circuit having a control output coupled to the trigger input and a command input coupled to the command bus, the delay circuit being responsive to the adjust command on the command bus to produce the control signal at a time corresponding to the adjust command.

14. The memory system of claim 13 wherein the phase comparator includes:

a signal source having a plurality of outputs and operative to produce a plurality of phase-shifted signals at the outputs in response to the master clock signal; and

a plurality of phase comparator, each phase comparator including a first input coupled to the signal source outputs, a second input coupled to the echo signal generator and a phase output coupled to the logic circuit.

15. The memory system of claim 14 wherein the signal source includes a multiple output delay-locked loop.

16. A method of adjusting data timing in a memory system having a memory device and a memory controller, the method comprising the steps of:

transmitting a first set of data to the memory device according to a first clock signal;

receiving the first set of data at the memory device;

establishing an initial output timing at the memory device having a default phase relationship with the first clock signal;

transmitting a second set of data from the memory device to the memory controller according to the initial output timing;

receiving the second set of data at the memory controller;

comparing the second set of data to the first clock signal in order to identify a phase error;

transmitting a third set of data from the memory controller to the memory device for revising the initial output timing in response to the identified phase error; and

revising the initial output timing at the memory device according to the third set of data to produce a revised output timing.

17. The method of adjusting data timing according to claim 16 wherein the step of transmitting a second set of data includes transmitting an echo clock signal.

18. The method of adjusting data timing according to claim 17 wherein the step of comparing the second set of data comprises the steps of:

generating a plurality of phase shifted signals responsive to the first clock signal;

comparing the echo clock signal to each of the phase shifted signals;

identifying one of the phase shifted signals having a phase within a selected range of phases relative to the echo clock signal; and

generating the third set of data according to the identification of the phase shifted signal.

19. The method of adjusting data timing according to claim 16 wherein the step of revising the initial output timing at the memory device includes the step of adjusting a vernier.

20. A method of adjusting data timing in a memory system having a memory device and a memory controller, the method comprising the steps of:

establishing an initial output timing at the memory device;

transmitting a first digital signal from the memory device to the memory controller according to the initial output timing;

receiving the first digital signal at the memory controller;

identifying a phase difference of the received digital signal relative to a timing reference signal;

transmitting an adjustment signal from the memory controller to the memory device for revising the initial output timing in response to the identified phase difference to produce a revised output timing;

revising the initial output timing at the memory device according to the adjustment signal; and

transmitting a second digital signal from the memory device to the memory controller according to the revised output timing.

21. The method of claim 20 wherein the step of identifying a phase difference of the received first digital signal relative to a timing reference signal comprises the steps of:

generating a plurality of phase shifted signals responsive to the timing reference signal;

comparing the first digital signal to each of the phase shifted signals; and

identifying one of the phase shifted signals having a phase within a selected range of phases relative to the first digital signal.

22. The method of claim 20 wherein the step of establishing an initial output timing includes the steps of:

setting a delay of a delay circuit; and

applying the timing reference signal to the delay circuit to produce the first digital signal.

23. The method of claim 22 wherein the step of establishing an initial output timing further includes the steps of storing data in an output register;

clocking the register with the first digital signal; and

outputting data from the register in response to the first digital signal.

24. The method of claim 22 wherein the step of revising the initial output timing includes the step of adjusting the delay of the delay circuit.